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Reliable Storage &
Embedded IoT Solutions

Quo vadis,
Chiplet AVT and Silicon Photonics?

Your trusted partner for reliably storing and protecting data in industrial and IoT applications.

Competence We Deliver

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Swissbit Production in Berlin, Germany

- Production and office Area 10.000m²
- Production area with clean room classes
- Production site in Berlin, Germany
- HQ in Switzerland
- 450 employees worldwide

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Memory Solutions

"Best Service Memory Company"

NAND Flash
Firmware & Tools
Optimization & Support

hyperstone®

"Most Reliable Controller"

Controller & Firmware
Tools & Customization
ODM Memory

Embedded IoT Solutions

Security Products
Firmware & Software
Sensors & Wireless

Advanced Packaging, Assembly & Test Solutions

IATF 16949 – ISO 9001 – ISO 14001 – ISO 27001 – ISO 50001

Made in Germany

Full control over the value chain! With our unique competencies, we reliably store and protect data in industrial, security and IoT applications.

Services We Provide: Custom Form Factor & System-in-Package

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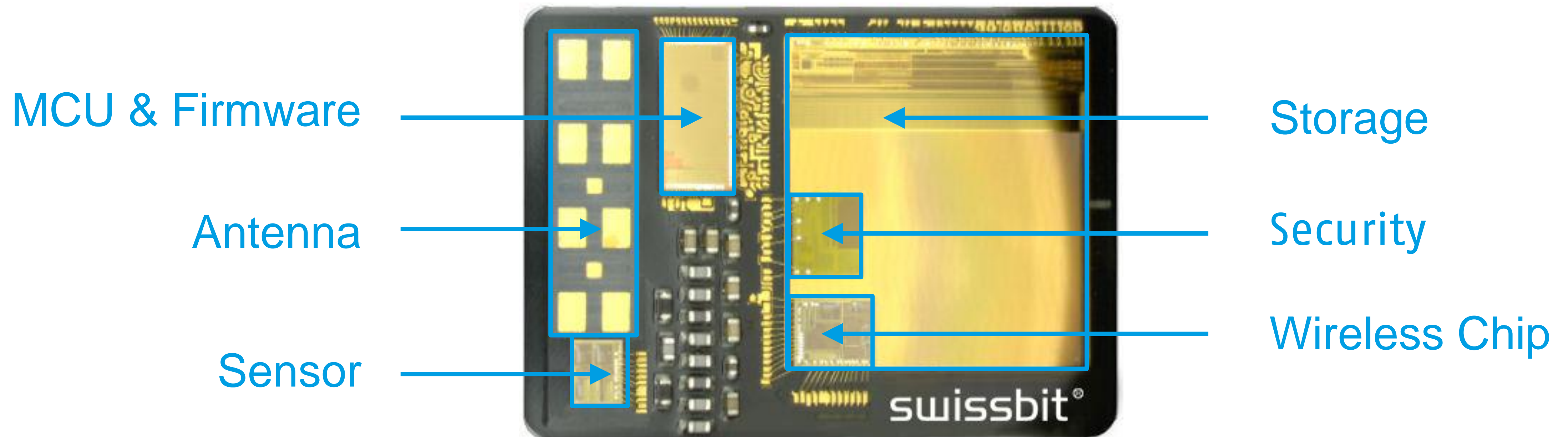
Swissbit Production in Berlin, Germany

Own production facility: We offer expertise in customer-specific system-in-package (SiP) for integrating various functionalities in a multi-chip package (MCP), as well as assembly and testing.



Various form factors: from secure microSD card to custom system-in-package

The 2.5 D SiP is a long-term stable process, the next challenges are CHIPLETS in a 3D SiP integration without silicon interposer.

Chiplet ECU System Building Blocks

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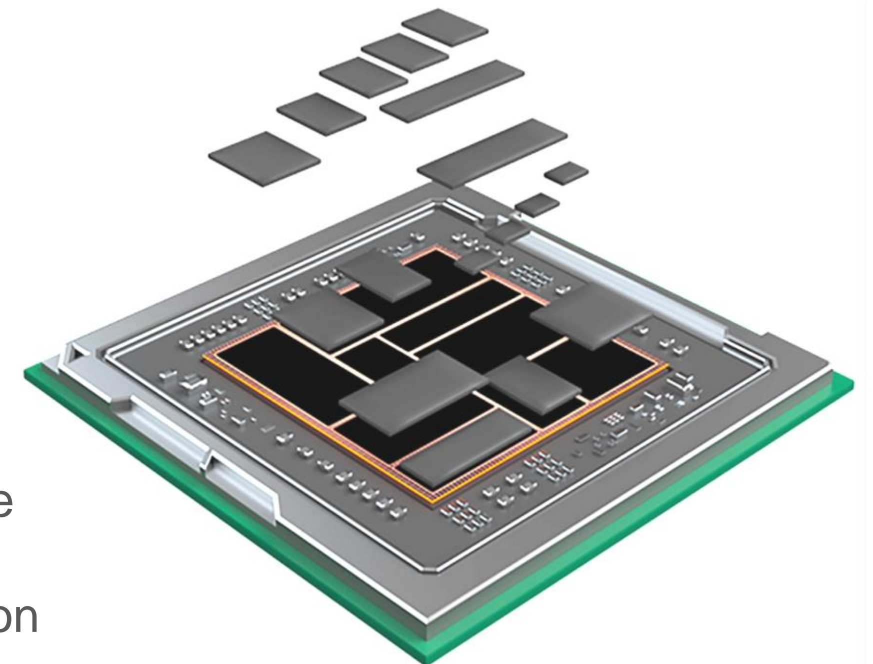
Intro

What is it about?

"More than Moore beyond Moore" is a technological and **disruptive process** at the center of which chiplet technologies are becoming essential for the success of heterogeneous **2.5 / 3D integration in AIoT / IIoT systems**, in the implementation of industrial solutions, strategies and ultimately suitable business models.

In the context of chiplets, new innovative infrastructure concepts are needed in AVT and DIE-to-DIE (D2D) communication modules.

Known B2B (board-to-board) or C2C (chip-to-chip) concepts are established specifically for manufacturers or promoted as open source and these are adapted to the SiP (system-in-package) problem. The previous concepts are very much tied to the available AVT and semicon node technology and are inflexible, energy-intensive (power per bit / I/O) and not suitable for heterogeneous integration without restrictions.



Wired :

- Bunch of Wire (**BoW**)
- PHY mit SerDes (**UCIe**)

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Chiplet Substrate buildup

The Smart Substrate for Chip Packaging

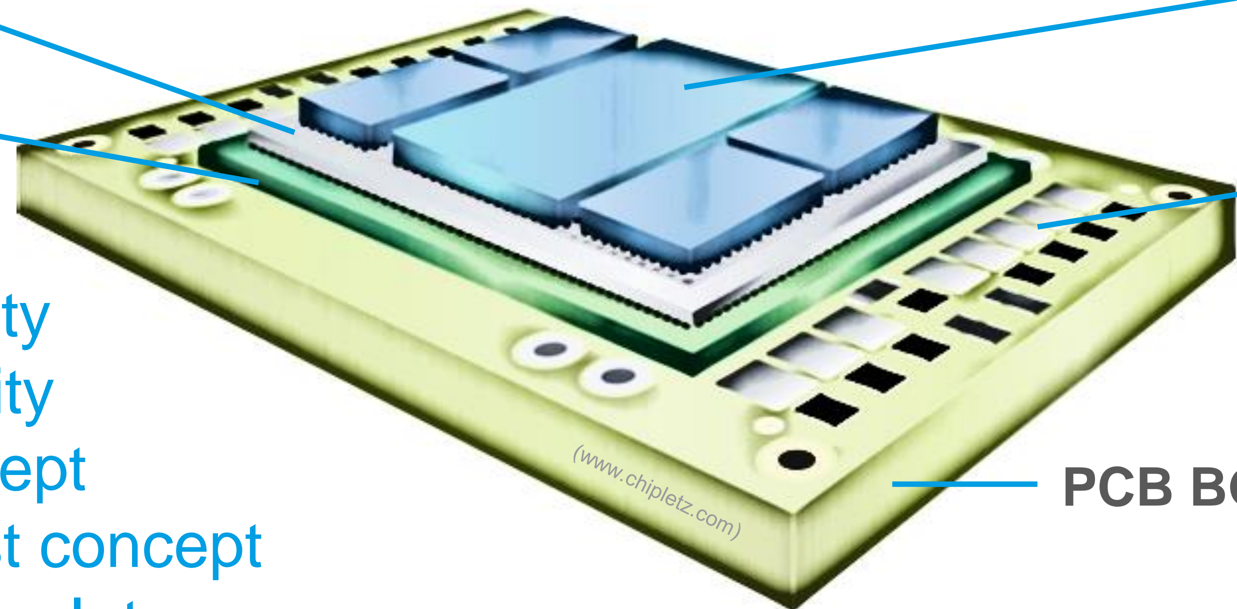
(Embedded Multi-DIE Interconnect Bridge (**EMIB**), Chip-on-Wafer-on-Substrate (**CoWoS**), Integrated-Fan-Out (**InFO**), System-on-Integrated-Chips (**TSMC-SoIC**) technologies)

Silicon Interposer

Organic Interposer

Chiplets – Flip Chips

Passive/active discrete Components



PCB BGA Fanout Board (RDL)

Challenges :

- Signal Integrity
- Power Integrity
- Cooling concept
- Multi DIE Test concept
- Without Silicon Interposer
- Availability of Organic Interposer

Heterogeneous integration of multi-DIE solutions in a system-on-package of different FABs and semicon nodes is the central idea of chiplets.

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Chiplet benefits

- higher Yield: Smaller chip sizes compared to monolithic SoC designs, better wafer utilization at the edges ($Yield_{SiP} = Yield^{N}_{Die} \times Yield_{Package} \times Yield_{Assembly}$)
- less Over Engineering: Optimization for specific functions/tasks (Analog IC, CPU, DSP, GPU, FPGA, RF, Photonics, etc.), adapted use of different semicon nodes/material (e.g. silicon, germanium, indium phosphide, gallium arsenide, gallium nitride, silicon carbide)
- low energy consumption in the package due to shorter connection paths between the chips compared to a board design
- More flexible product development through modularity and reuse of existing designs at the package level, reducing the risk of demanding SoC development
- shortens design time, shortens the time-to-market of individual system solutions
- smaller risk in chip design: Cost reduction through shortened design time, better yield, free choice of semicon nodes/materials

Goal: Multivendor chiplet ecosystems, for cost-effective specialized hardware in modern workloads with system-in-packages (SiP) solutions, as “drop-in chiplets” in a chip package (**form-, function-, power-, cost-fit**) e.g. for certified products with fixed BOM.

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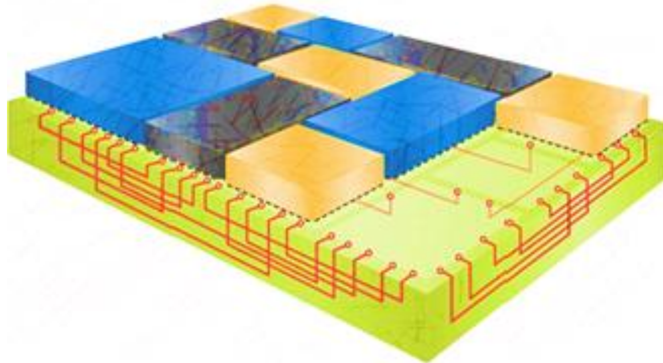
Chiplet Substrate – Package / Chip PCB – Package Systemdesign

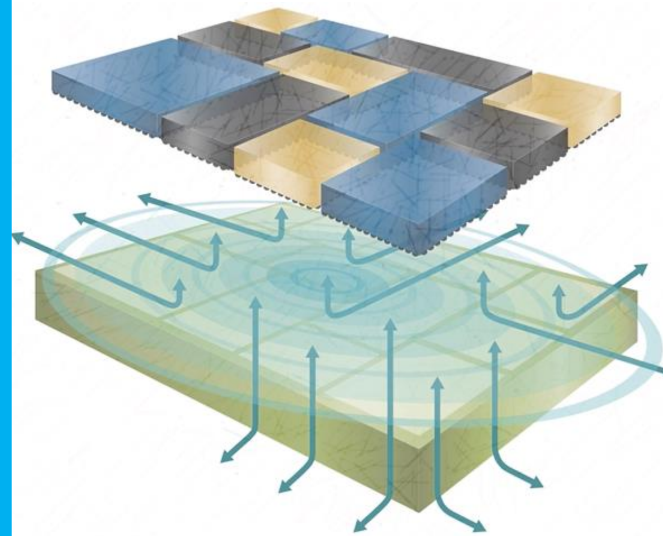
DIE-to-DIE (D2D) interconnect in the substrate

New with Chiplet technology



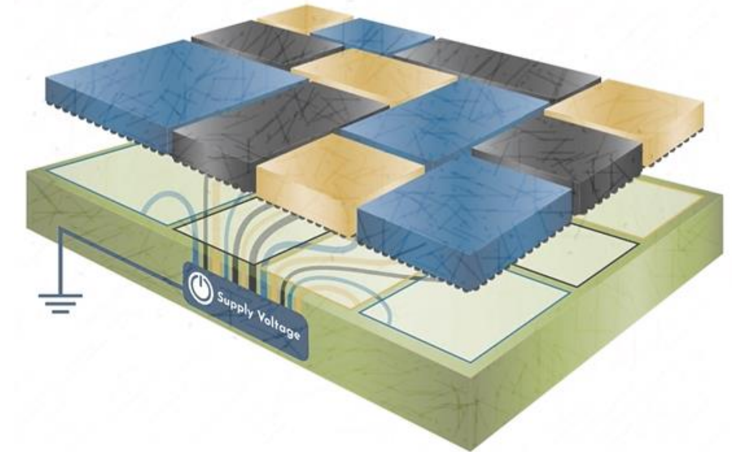
Universal Chiplet Interconnect Express (**UCIe**), Advanced Interface Bus (AIB), Bunch of Wires (**BoW**), Open Domain-Specific Architecture (ODSA), and Open High Bandwidth Interface (OHBI)

RDL - High-speed I/O from the substrate



High Speed I/0 : PCIe Gen4 to Gen6, SATA, USB 3.x, USB 4.x, LPDDR4 / 5 SDRAM

Support for different voltage domains across the substrate from a single/dual power supply



Core Voltage / I/O Voltage
High current / low voltage :
3W to 200W at 0.8V to 0.5V
LDO / DCDC Converter - PMIC

State of the art without chiplets

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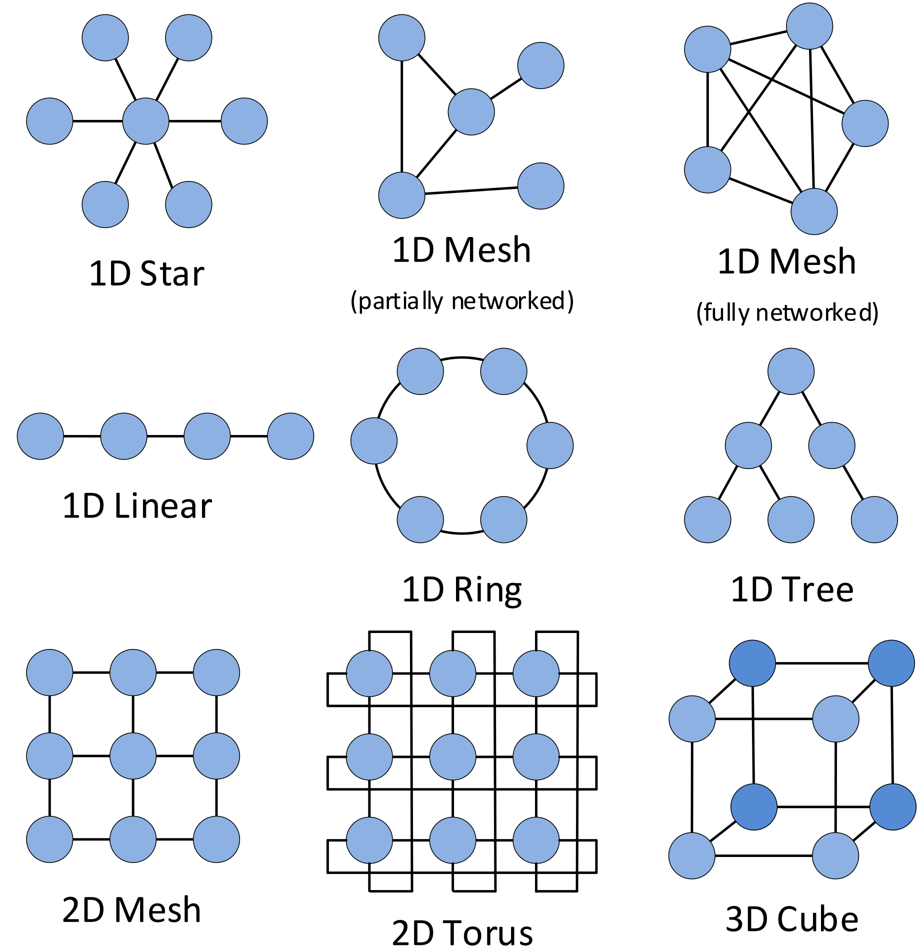
DIE-to-DIE interconnects – bus systems

Depending on the system requirements regarding functional safety and cybersecurity, the chiplets (depending on the number) in a SiP can be connected in different network topologies (including mixed network topologies) that support system-specific data flows or security concepts (e.g. separation, redundant paths , strict processing chains, etc.).



The D2D chiplet network topology follows from the function or data flow model.

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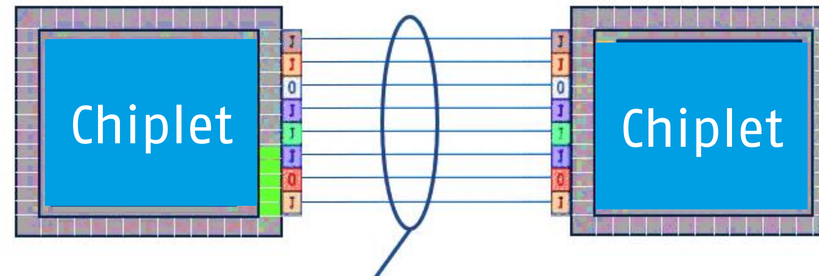
State-off-the-Art wired Die-to-Die Interface Technologies – Chiplets differentiation

BoW – parallel Interface:

- many signal lines
  (ca. 1 Tb/s ca. 2.048-4.096)
- low latency < approx. 1ns
- low energy requirement per signal



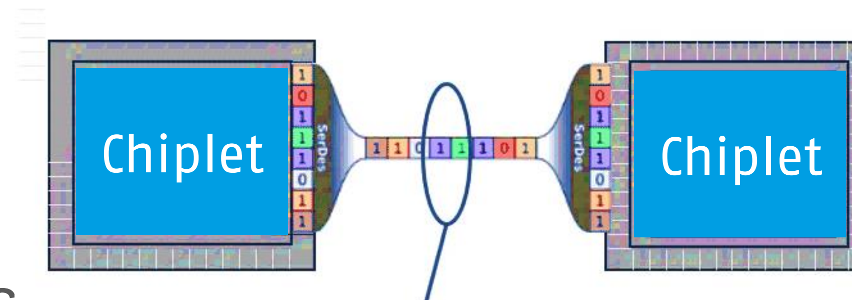
digital IO frequencies typically have a **frequency barrier** of approx. **1 to 5 GHz**

typ. 1 - 2,5 GHz / Signal
max. 1 - 5 mm Wire length
typ. bump pitch 35 - 150 µm

Stern-Topologie (4 Chiplets)
3x 2.048-4.096 Wires
1x 6.144-12.288 Wires

UCIe – serial Interface:

- few differential signal lines
  (approx. 1 Tb/s approx. 32 lanes)
- higher latency < approx. 10ns
- higher energy requirements per lane



Electric serial bus systems typically have a **data rate barrier** of approx. **150/250 Gb/s**

typ. 16 - 32 Gb/s / Lane
max. 10 - 25 mm Lane length
typ. bump pitch 35 – 150 µm

Star-Topologie (4 Chiplets)
3x 32 Lanes each with 32 Gb/s
1x 96 Lanes each with 32 Gb/s

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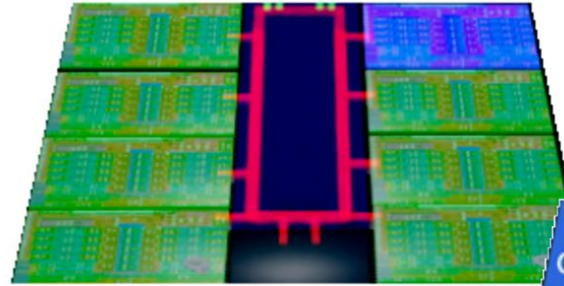
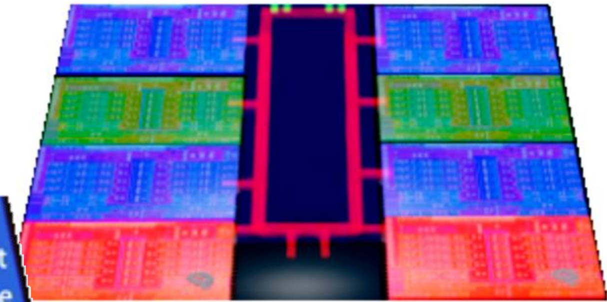
HPC - Chiplet Substrate – PCB – Package system design

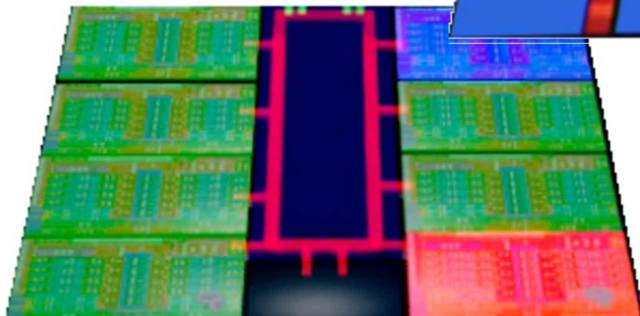


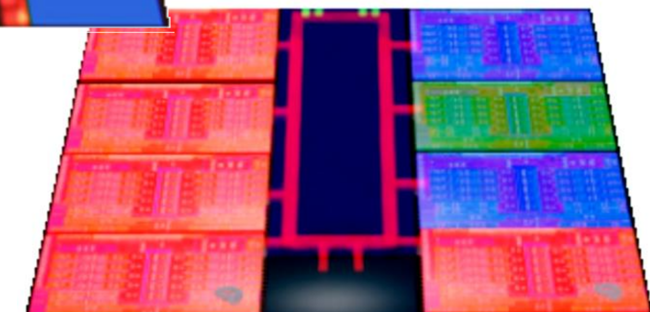


Modular platform,
Chiplet-based using UCIe IF

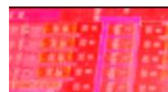
BoW-Star topology
(13 Chiplets)
12x 2.048-4.096
1x 24.576-49.152

UCIe-Star topology
(13 Chiplets)
12x 32 Lanes je 32Gb/s
1x 384 Lanes je 32Gb/s





Chiplet geometry selection help to change the computing profile


Machine Learning

FPGA or ASIC

CPU or DSP

Chiplet ECU System Building Blocks

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Reusable generalizable heterogeneous integration of chiplets?

- BoW Technology parameters force a very precise arrangement of the IO pads
  - primarily suitable for silicon interposers
- UCIe Technology parameters limit the usable number of chiplets
  - favored technology for organic interposer (IC UHD organic substrate material)
- BoW and UCIe extremely increase the design complexity of interposers
  - Wiring density in the interposer, signal and power integrity, reliability
- Chiplets with BoW and UCIe technology limits the generic reuse of the chiplets
  - geometric positioning specifications, Warpage and hotspots problems
- The electrical D2D chiplet interface technologies (BoW, UCIe) in version 1.x already have recognizable bandwidth barriers (physical limits)
  - In the world of communications, the transition from electrical to optical data transmission took place over a decade ago.
- Non-generalizable / reusable network topology, including the functional and data flow models, are very difficult or impossible to implement with chiplets
- The UCIe and BOW standards currently offer no support with regard to design and supply chain security (as of Q3/2023)

Design nightmare / killer criteria / special solutions?

Chiplets – a new opportunity of silicon photonic

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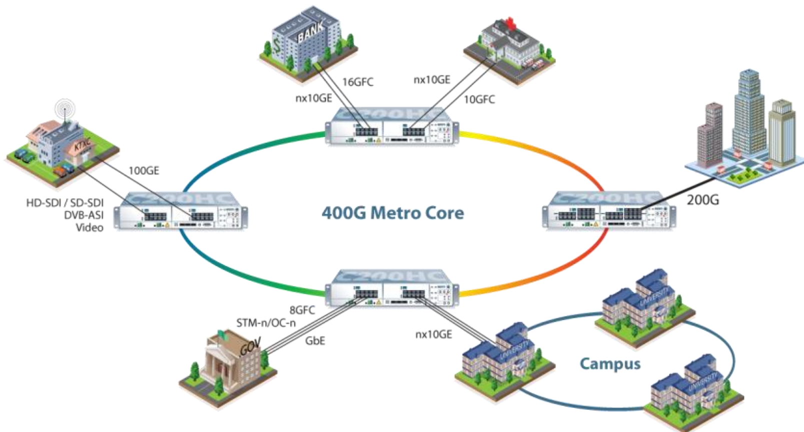
Evolution of Photonic and Silicon Photonic systems

1. Photonic application era

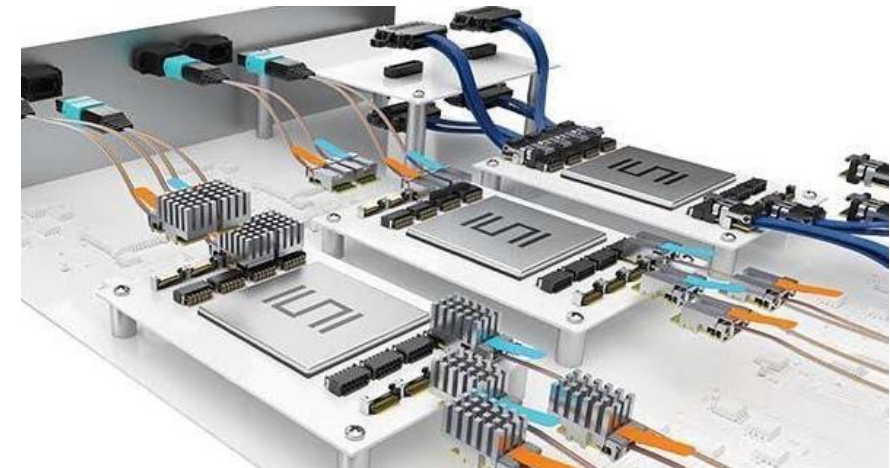


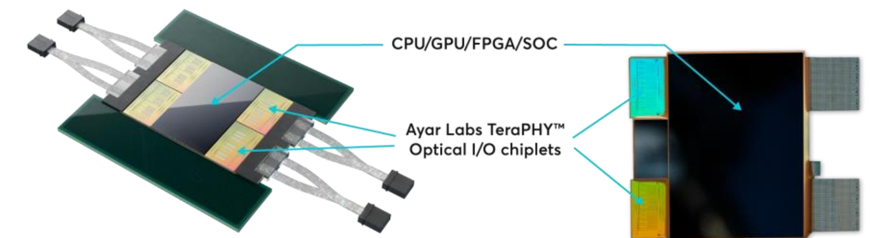
Metro networks (MAN / WAN)

2. Photonic application era

Data center networks

3. Photonic application era



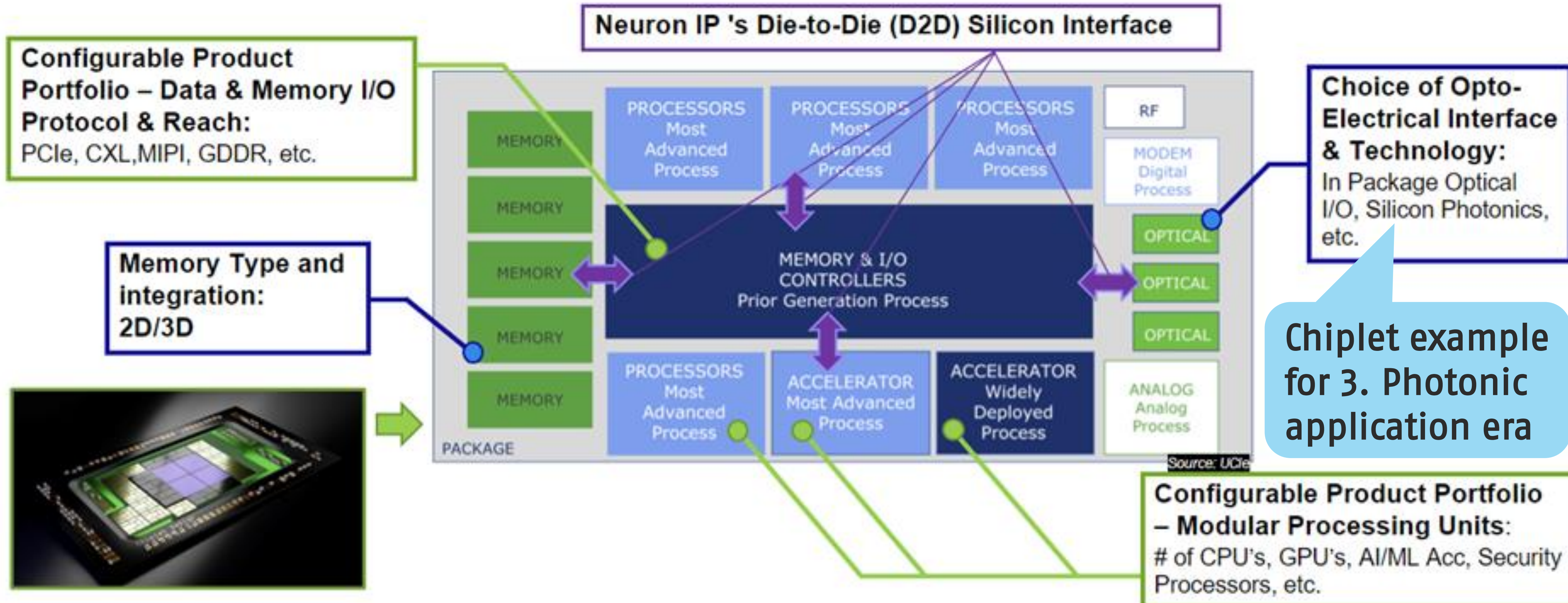


Chip2Chip networks in data center components

The driving force for Silicon Photonic are large language models like ChatGPT. Silicon Photonic is already being used, for example in optical transceivers for transmitting high data rates in data centers.

Chiplet – a new opportunity of silicon photonic

NEURON IP – UCIe Version 1.1



Chiplets – a new opportunity of silicon photonic

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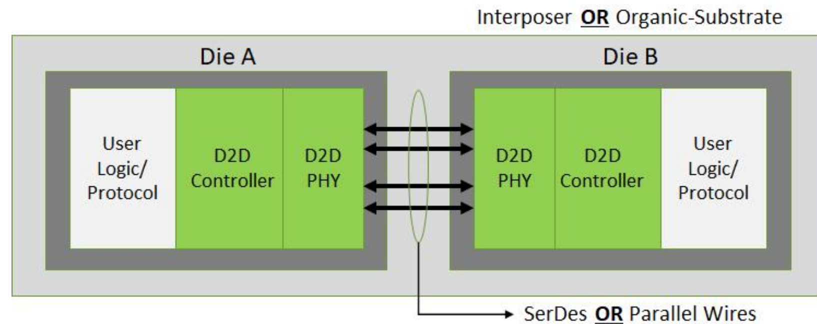
Evolution of Photonic and Silicon Photonic Systems

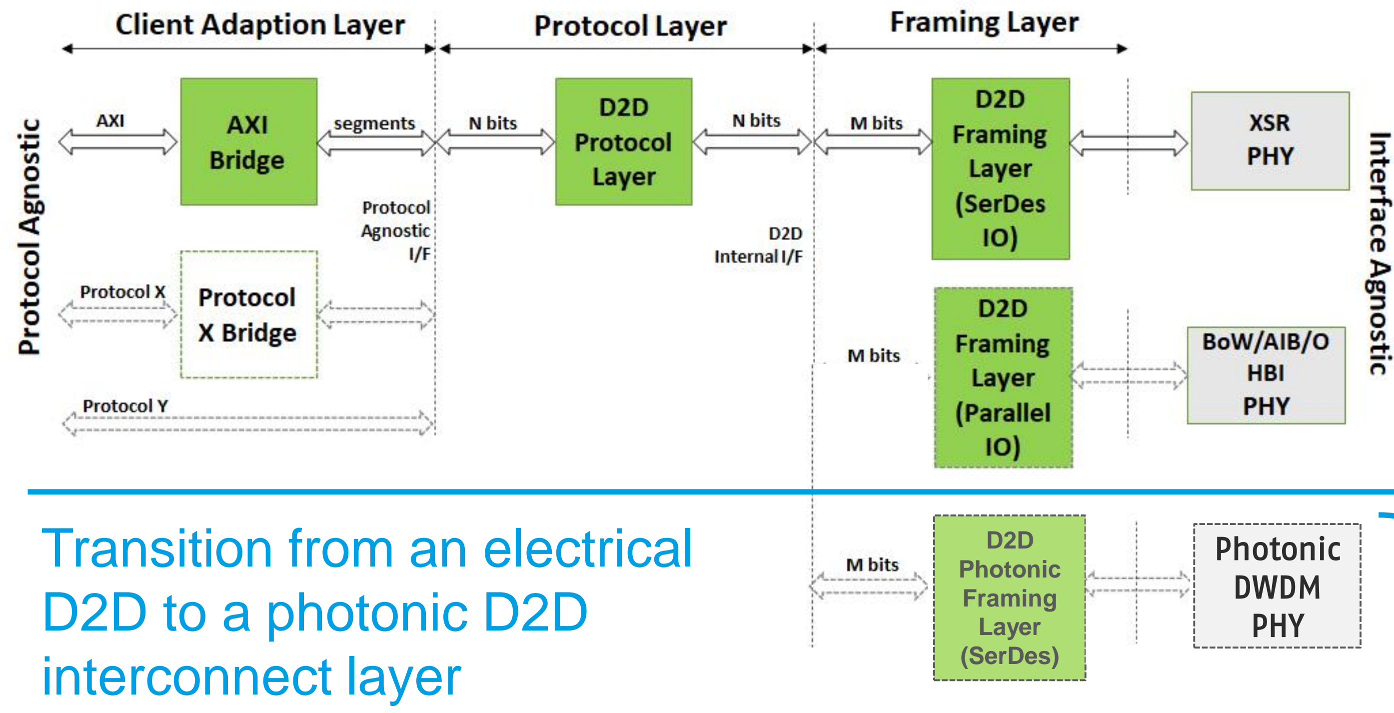
4. Photonic application era



Silicon Photonic refers to the integration of photonic and electronic components on one chip. “If we provide a good silicon integration system, we can both reduce the power consumption of AI chips and increase their computing power,” said Douglas Yu, vice president of pathfinding for system integration at TSMC, on the sidelines of SEMICON Taiwan: » This is a paradigm shift, we are at the beginning of a new era.«

The IO requirements of AI/ML systems require optical technical innovations. Co-packaged Photonic D2D interconnects are the best candidates to meet the energy efficiency and bandwidth scaling requirements of these systems

- Tighter electrical-optical integration to support lower power consumption
- WDM architectures appear to overcome the challenges of BW density
- Companies like Intel, AMD, Cisco, IBM, Nvidia and Huawei have been working on Silicon Photonics for many years.



Transition from an electrical D2D to a photonic D2D interconnect layer

TSMC COUPE
(Compact Universal Photonic Engine)

Chiplets – a new opportunity of silicon photonic

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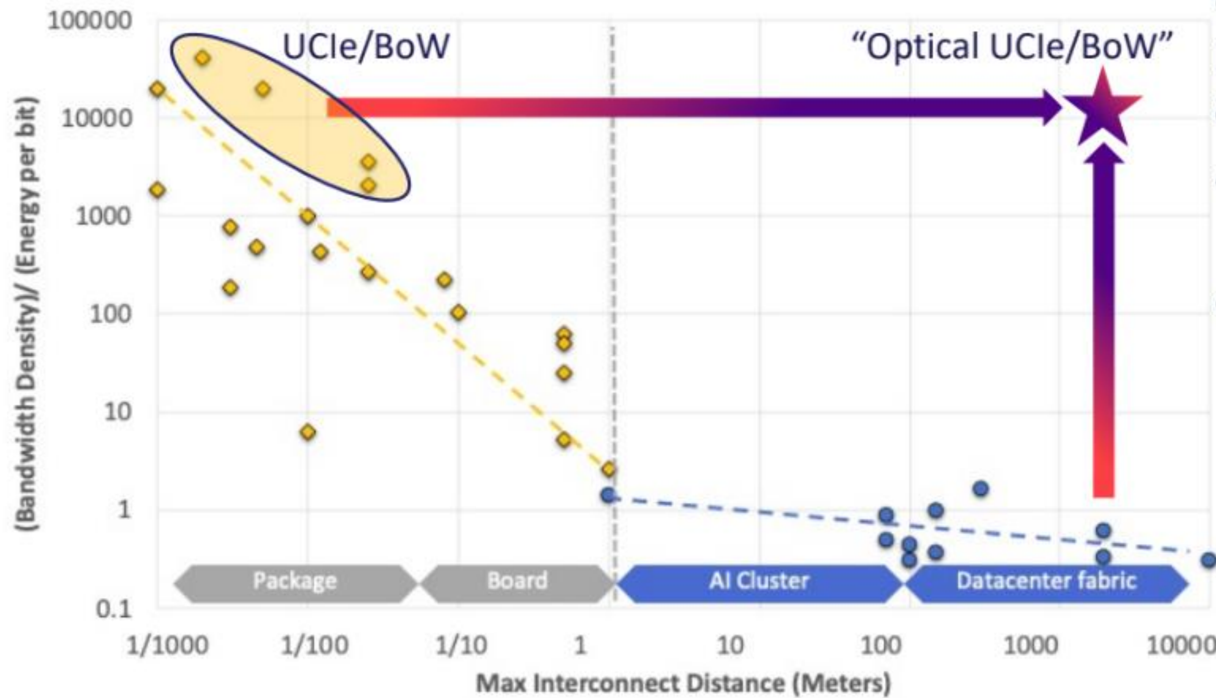
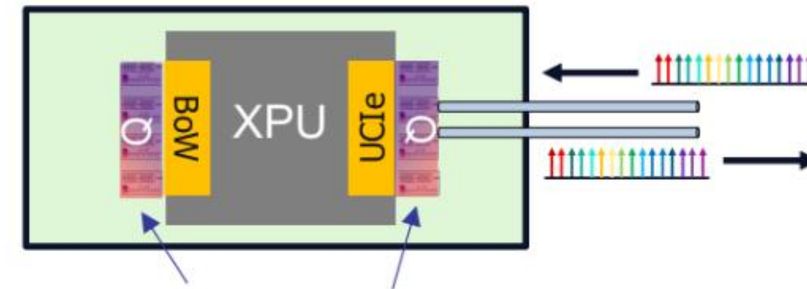
Research project – OCP 18-20.10.2022 Scaling optical connectivity with DWDM silicon photonics

UCIe/BoW-over-fiber



"Optical UCIe/BoW" chiplets extending low latency + low power "die-to-die" like connectivity across the datacenter

- DWDM enables 1:1 "wavelength-to-pin" mapping to preserve low latency & low power
- UCIe capacity over a single fiber: 64 lanes x 32 Gbps NRZ → 64 wavelengths @ 32 Gbps per λ



Optical UCIe/BoW chiplets

Optical compute interconnects (UCIe/BoW, CW-WDM)

Higher bandwidth per fiber, simple signaling to reduce power & latency

Challenge: Wavelength generation/control & PIC implementation

Photonic Interface Performance:

- typically approx. 1 lane 100 Gb/s to 1 Tb/s
- Up to 1000 Tb/s are now technically possible via fiber optics

Chiplets – a new opportunity of silicon photonic

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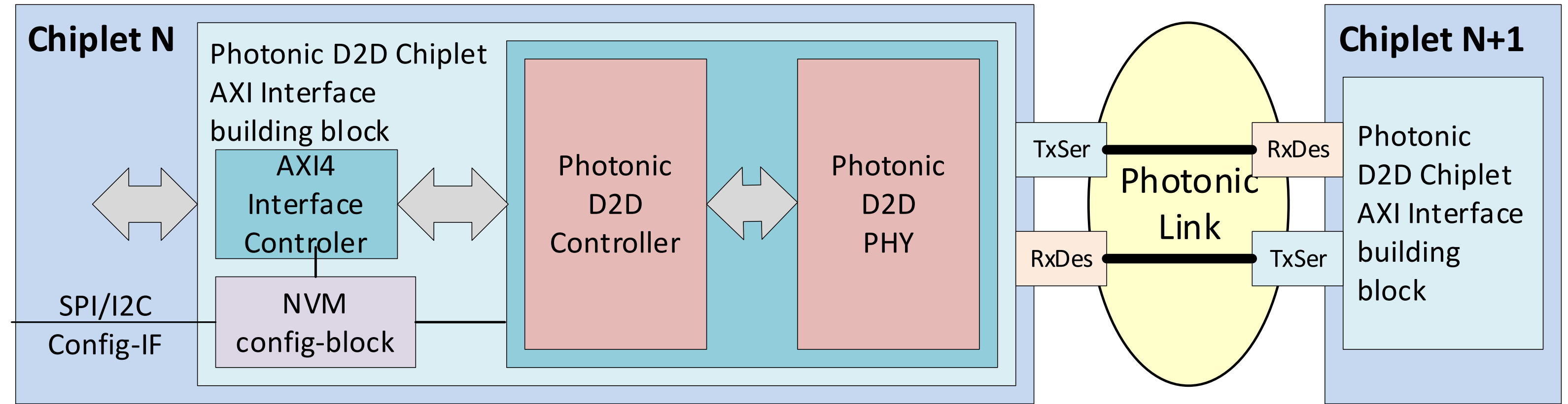
Chiplet Photonic Interface building block (Challenges)

D2D Photonic Link on a new interconnect layer



- Complete integration of the Ultra Short Photonic Link in the same CMOS process for the chiplets (scalable from < 10nm to 130nm semicon nodes, e.g. GF 22nm FDX, IHP 130nm)
- All D2D data communication takes place via single photonic links in a separate wiring level via optical waveguides (optical bridges)
- Future viability of the bandwidth approx. 1 Tb/s to 1000 Tb/s, no bandwidth barriers relevant today
- Design freedom for RDL - high-speed I/O from the Organic Interposer, power and signal integrity are comparable to the state of the art
- Generalizable / reusable network topology, including functional and data flow models

Chiplets – a new opportunity of silicon photonic

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Chiplet Photonic D2D Interface building block features

Physical Factors	Copper D2D Interface	Photonic D2D Interface
Flammability	electricity, short-circuit, heating	No electricity, no self-heating
Corrosion	Oxidation, toxic	No corrosion, non-toxic
Routing	length restrictions	no limitations
Bending	no limitations	Limitations (waveguide radii)
Size and Weight	High	Low
Cost	Low	Packaging: Medium; Maintenance: Low
Transmission Factors	**Copper D2D Interface**	**Photonic D2D Interface**
Bandwidth	Low	High
Interference, Crosstalk	susceptible	secure
Power Consumption	High	Low
Design Factors	**Copper D2D Interface**	**Photonic D2D Interface**
IC Substrate	Silicon Interposer, IC organic substrate	embedded waveguide
Design-In	extremely complex	reduce complexity / new challenges
freedom of design	very Low	High

NEW CHALLENGES

Chiplets – a new opportunity of silicon photonic

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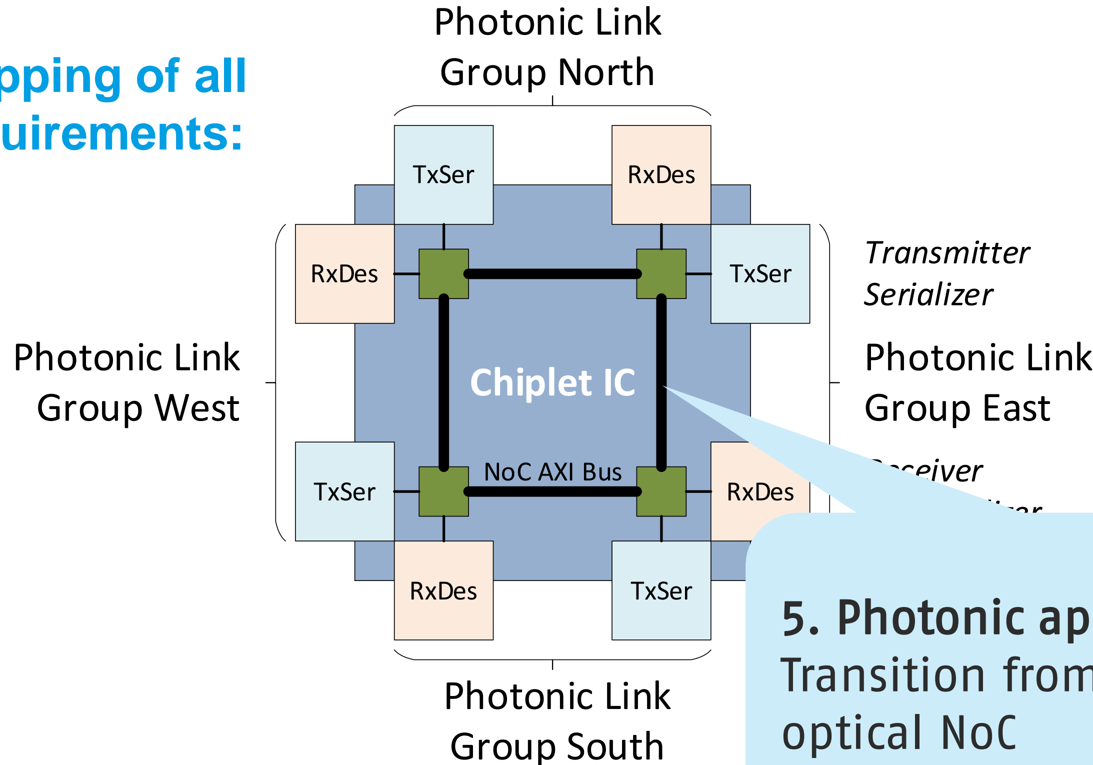
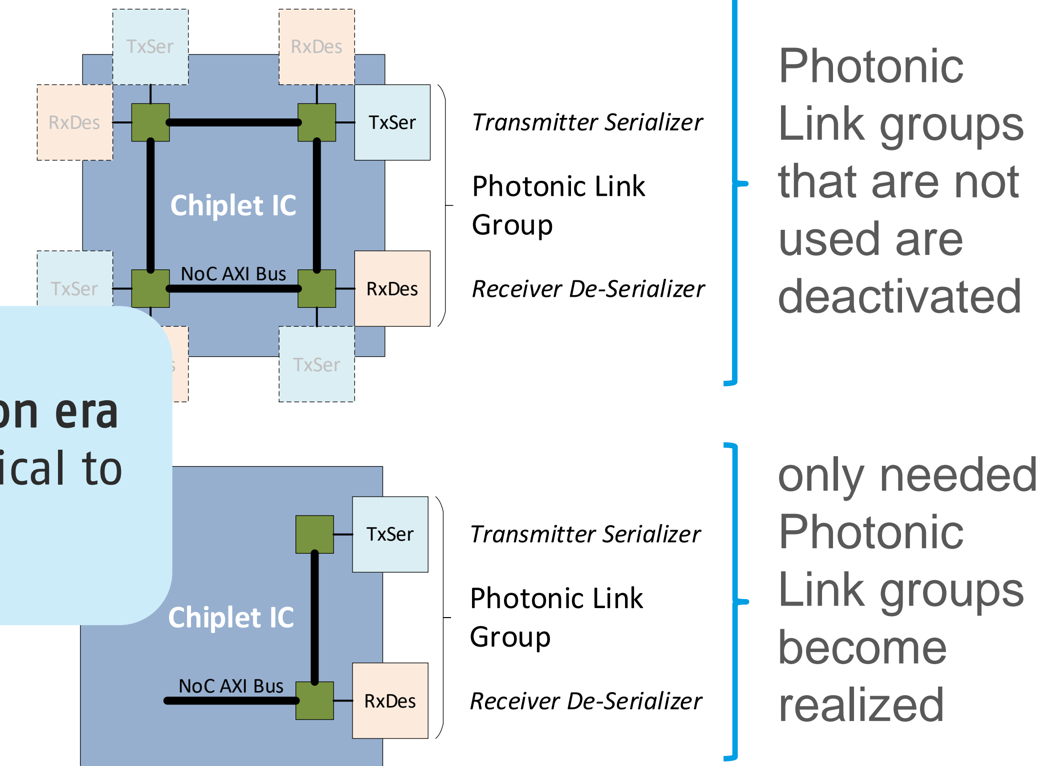
Chiplet Network-on-Chip (NoC) Core Building Block (physical view) with Photonic DIE-to-DIE (D2D) Interface

Mapping of all requirements:



5. Photonic application era
Transition from electrical to optical NoC

Illustration of minimum requirements:



Photonic Link groups that are not used are deactivated

only needed Photonic Link groups become realized

Implementation options of SerDes Groups

RxDes
TxSer

Options:

- Bunch of Wire Link
- Wired SerDES Link
- Ultra short Photonic Link

} Standard Interfaces

⟵ *innovative process*

Chiplet Application - System Building Blocks

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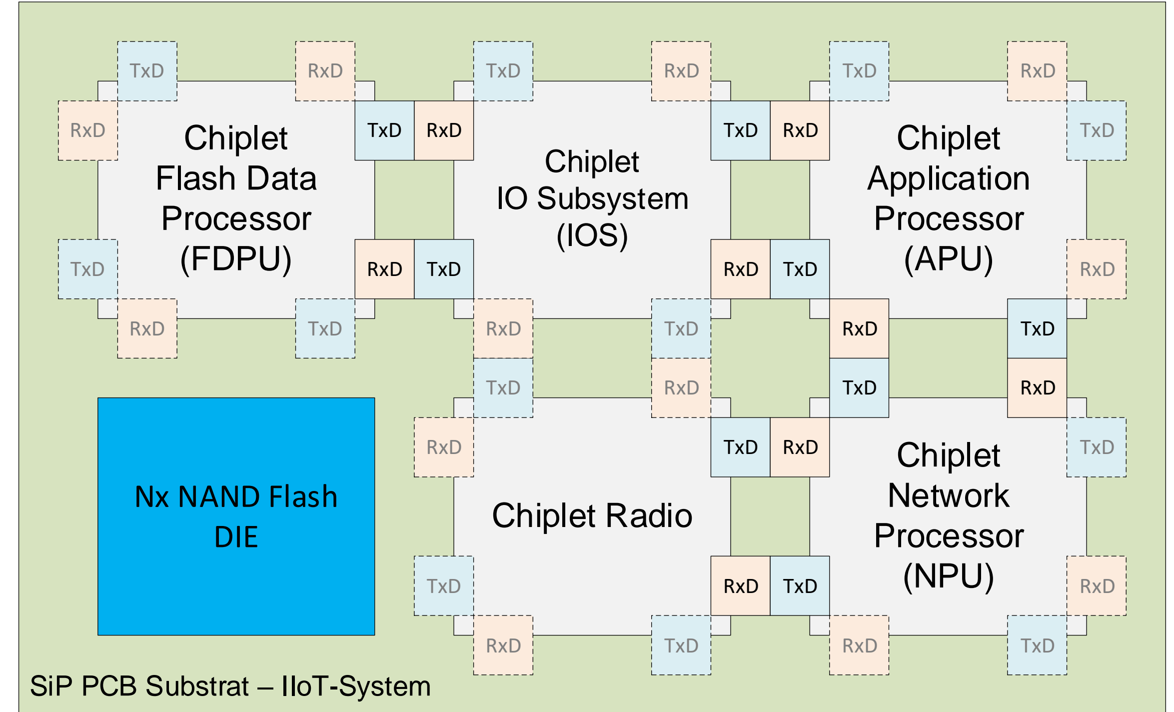
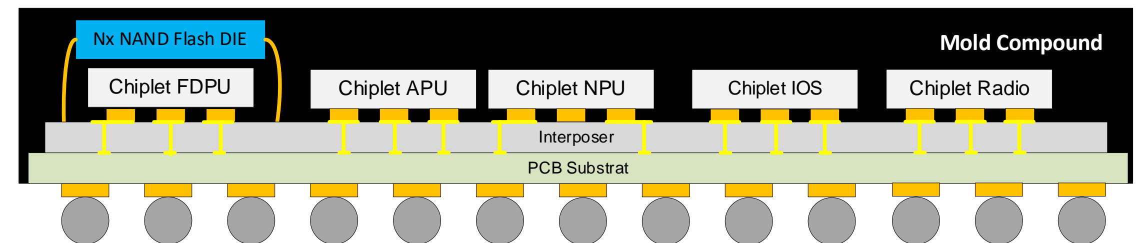
Chiplet NoC Core Building Block (assembly view)

TxSer
RxDes
Chiplet IC
NoC AXI Bus
Substrate corner bus ring
Chiplet NoC AXI bus ring

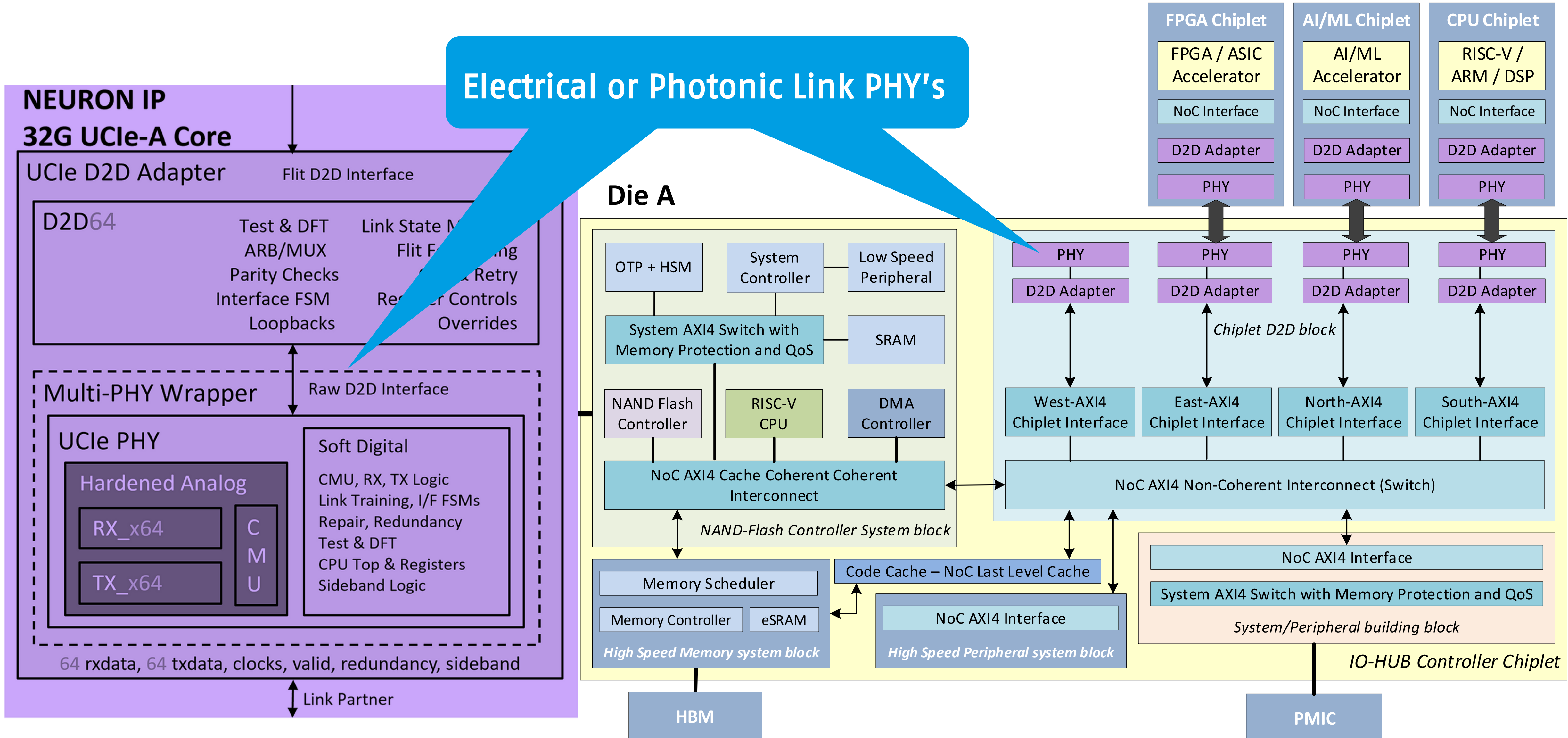




hierarchical SerDes / Photonic Link rings with closed and open data communication between chiplet DIE and the organic interposer

Chiplet Application - System Building Blocks

Chiplet System Chip Architecture (system view)



Chiplet – D2D Photonic Link

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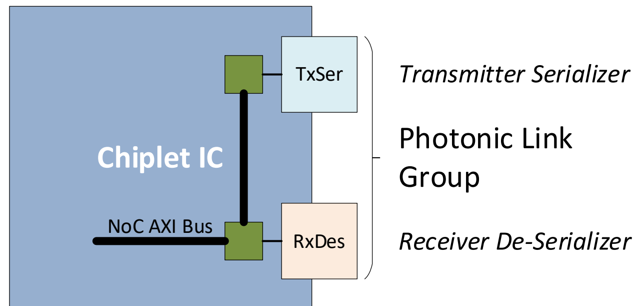
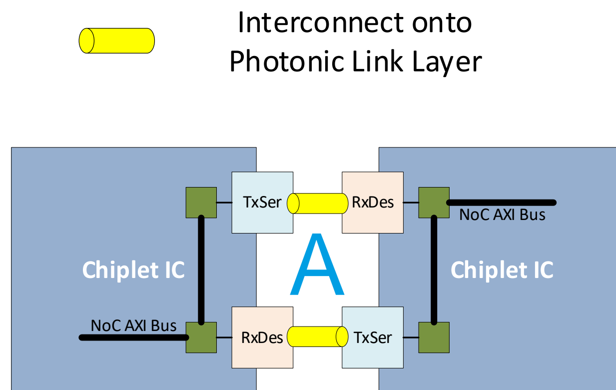
Evolution Steps for PoC – Demonstrator Module

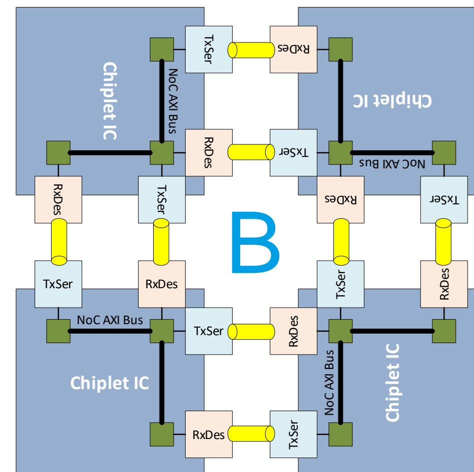


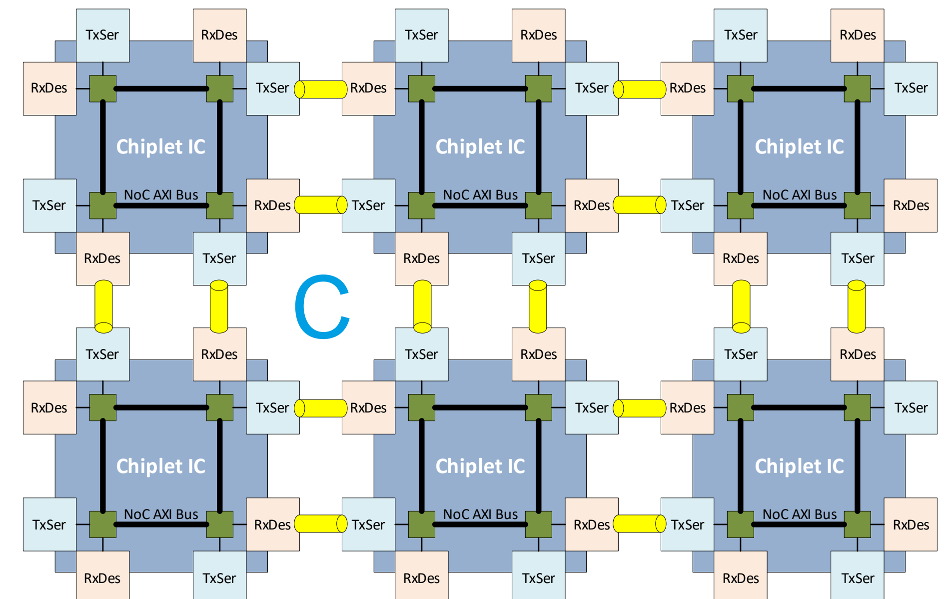
What steps can be used to set up a D2D Photonic Link in a demonstrator?

Demonstrator 3D Advanced Packaging Steps

A. 2 x DIEs on Chip – 1 Photonic Link via DIE
B. 4 x DIEs on Chip – 2 Photonic Link via DIE
C. 6 x DIEs on Chip – 4 Photonic Link via DIE







Chiplet – D2D Photonic Link

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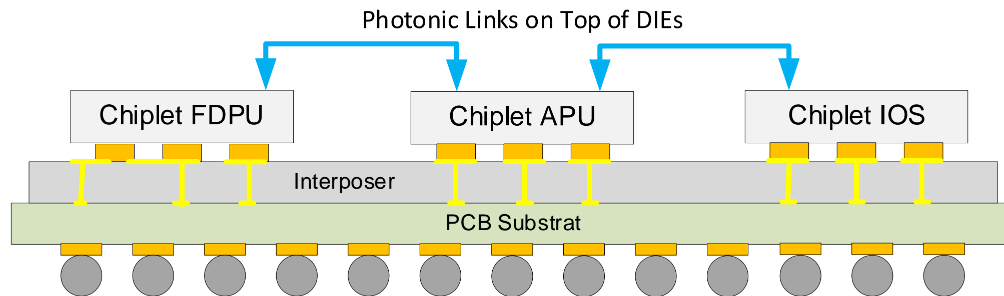
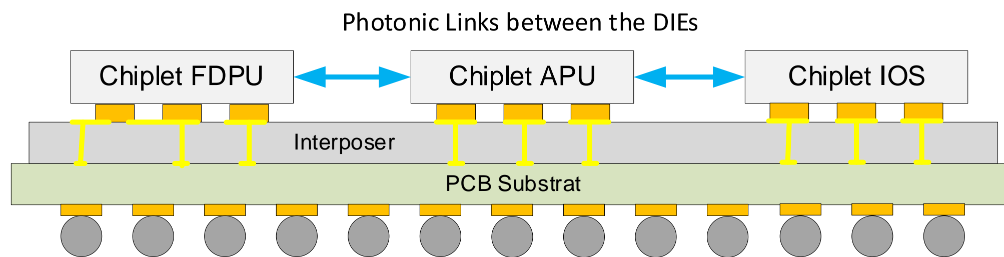
Evolution Steps for PoC – D2D Photonic Link Layer

How is the photonics link layer constructed in 2.5D/3D advanced packaging?



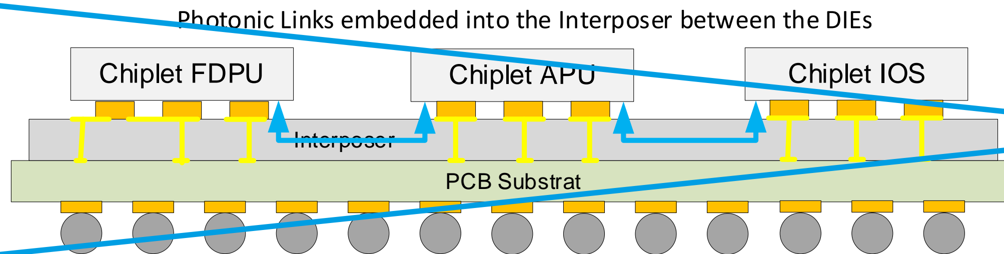
This variant would be possible in principle because it does not change the complexity of the interposer or PCB substrate and inserts a new photonic wiring layer. Optimal for the window molding process and brings additional requirements for heatsink connections.

Prio2



This variant is preferable because it does not change the complexity of the interposer or PCB substrate and inserts a new photonic wiring layer. Optimal for the window molding process and makes better use of the space between the DIEs, more optimal for heatsink connections.

Prio1



This variant should in principle be avoided as it increases the complexity of the interposer or PCB substrate, not a question of feasibility. Solution should be kept free for chip-to-chip via board PCB.

Prio3

Chiplet – D2D Photonic Link

Evolution Steps for PoC – Top View Structure

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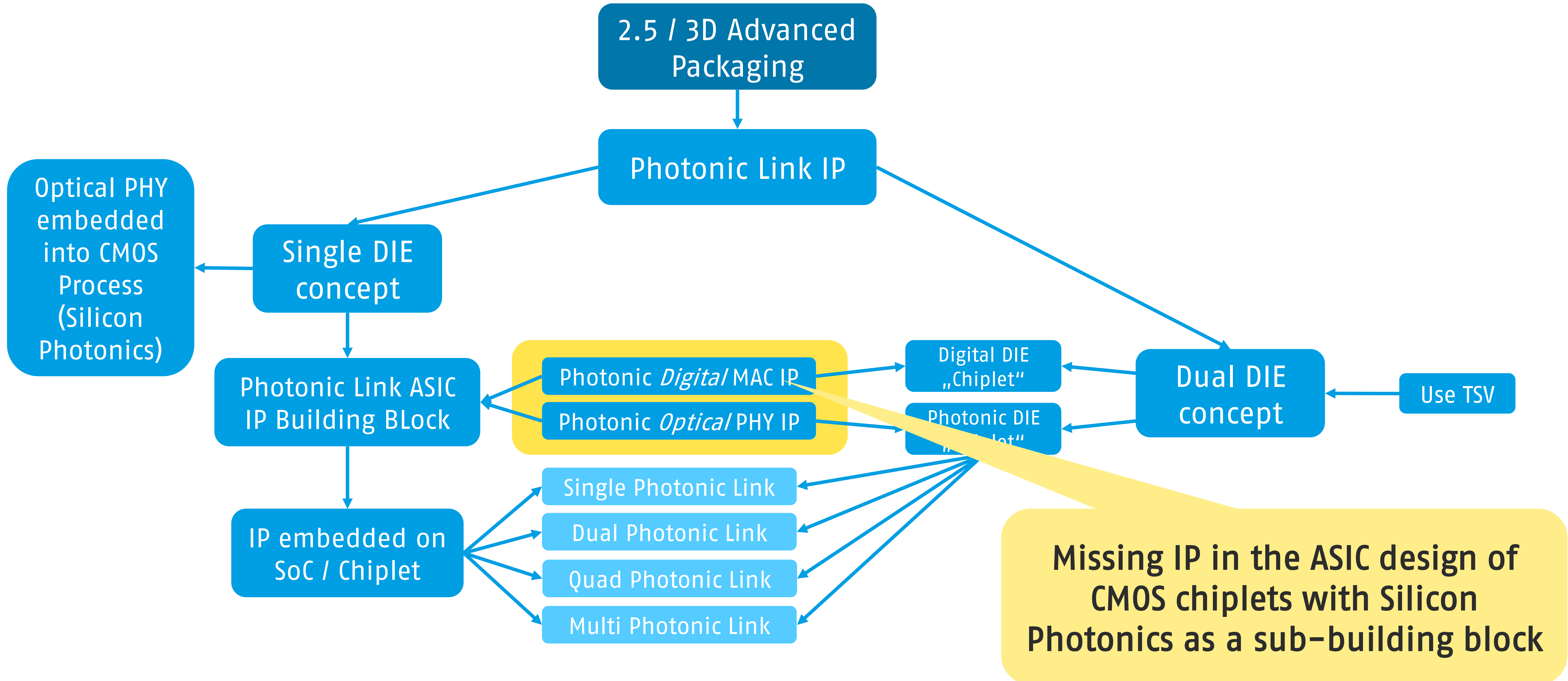

Chiplet – D2D Photonic Link

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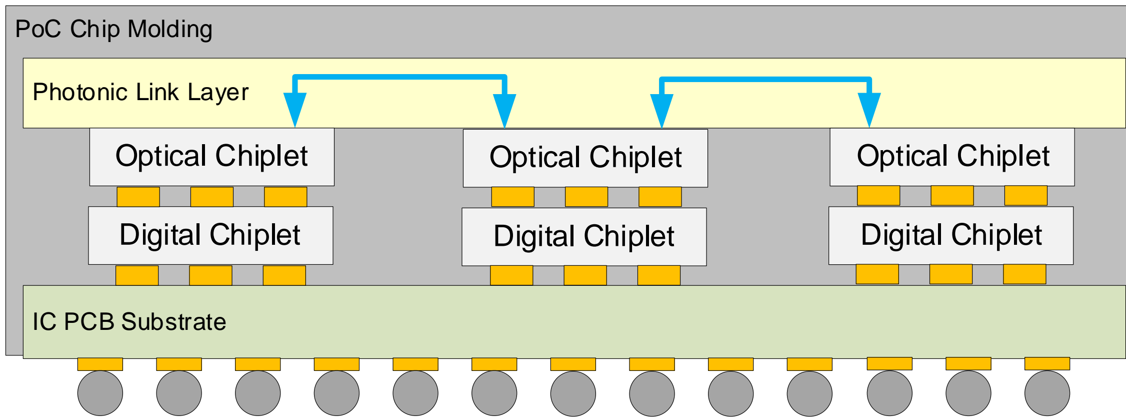
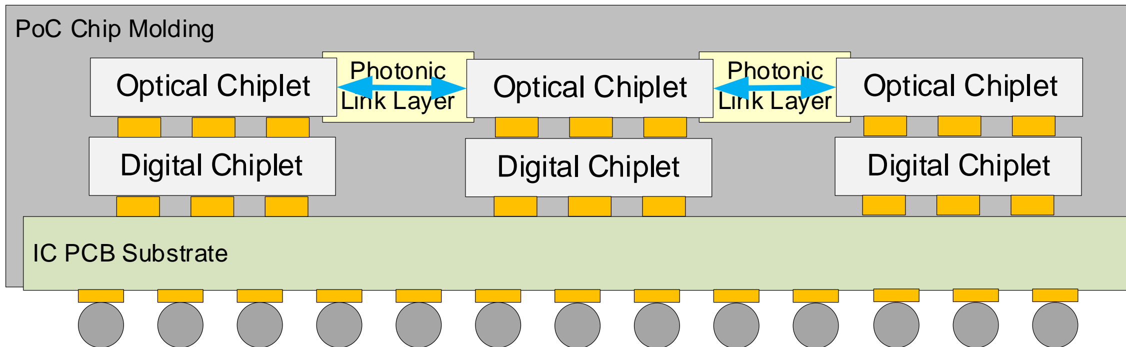
Exploring the Dual DIE PoC Chip Concept

Prio3



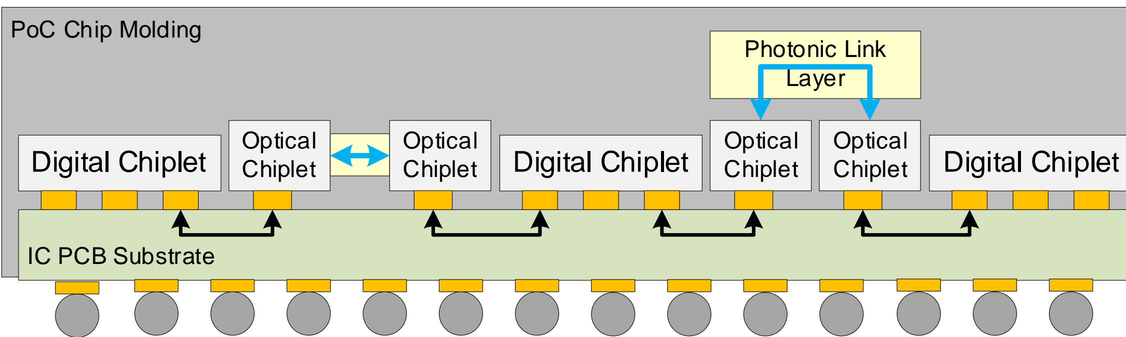
Photonic Links on Top of DIEs

Prio2

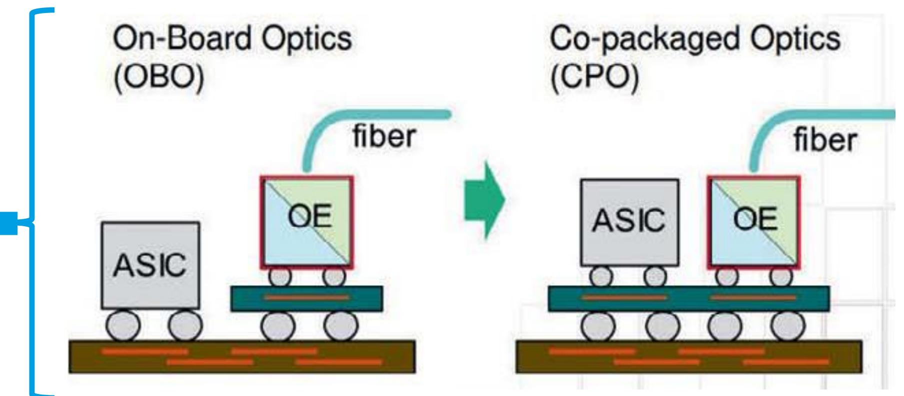


Photonic Links between DIEs

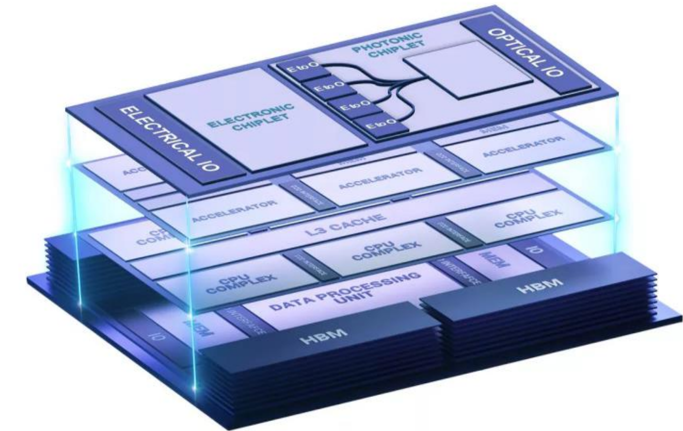
Prio1



Photonic Links in the same plane of DIEs



State of the art technology



Future construction technology

Optical Chiplet = TIA
PIC (Photonic Integrated Chip)
PIC = Optical Chiplet + Digital Chiplet

Chiplet Applications – a new opportunity of silicon photonic

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Summery

- System on Package mit Chiplets: The New „Configurable“ SoC Platform !
- “More than Moore beyond Moore” is a technological and disruptive process centered around chiplet technologies
- D2D technologies are the enablers for “More than Moore beyond Moore”
- D2D Chiplet technologies and Silicon Photonics are symbiotic (like PCIe & Ethernet in terms of performance and bandwidth)
- missing **Photonic** digital MAC- & optical PHY- **IP** for ASIC Design
- Substrates + AVT + Chiplets must be viewed holistically in design & semiconductor backend manufacturing

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Torsten Grawunder / Senior System Designer

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