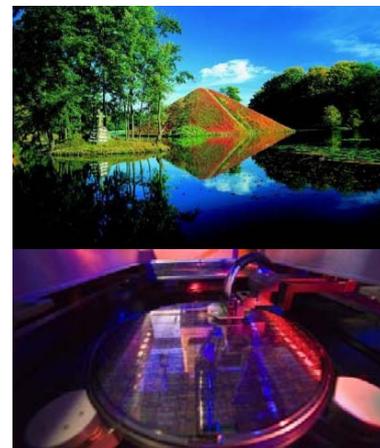




# 14<sup>th</sup> IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems

Brandenburg University of Technology Cottbus  
and Leibniz Institute for Innovations for  
High-Performance Microelectronics (IHP)  
in Frankfurt (Oder), Germany

April 13-15, 2011



<http://ddecs2011.informatik.tu-cottbus.de>

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## Call for Papers

The **IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems** provides a forum for exchanging ideas, discussing research results, and presenting practical applications in the areas of design, test, and diagnosis of nanoelectronic circuits and systems. The symposium also offers an insight into relevant European R&D collaborative programs, projects, and technology platforms.

The **DDECS Symposium** series has been organised by Central European countries: Czech Republic (1997, 2002, 2006, 2009), Poland (1998, 2003, 2007), Slovakia (2000, 2004, 2008), Hungary (2001, 2005), and Austria (2010).

DDECS 2011 is organised by **Brandenburg University of Technology Cottbus** and the Leibniz Institute **IHP - "Innovations for High-Performance Microelectronics"** in Frankfurt (Oder), Germany. The symposium is sponsored by the **IEEE Computer Society Test Technology Technical Council (TTTC)**.

### Topics of interest include but are not limited to:

- |   |   |
|---|---|
| <input type="checkbox"/> ASIC and SoC Design                  | <input type="checkbox"/> Analog, Mixed-Signal, and RF Test      |
| <input type="checkbox"/> FPGA Design                          | <input type="checkbox"/> SoC Test                               |
| <input type="checkbox"/> Bio-inspired Hardware                | <input type="checkbox"/> Built-in Self-Test and Self-Repair     |
| <input type="checkbox"/> Design Verification/Validation       | <input type="checkbox"/> Design for Testability and Diagnosis   |
| <input type="checkbox"/> Formal Methods in System Design      | <input type="checkbox"/> Defect/Fault Tolerance and Reliability |
| <input type="checkbox"/> Hardware/Software Co-Design          | <input type="checkbox"/> On-line Testing                        |
| <input type="checkbox"/> IP-based Design                      | <input type="checkbox"/> Embedded Systems Testing               |
| <input type="checkbox"/> Logic Synthesis                      | <input type="checkbox"/> Memory, Processor Testing              |
| <input type="checkbox"/> Physical Design                      | <input type="checkbox"/> MEMS Testing                           |
| <input type="checkbox"/> Design and Test in Nano-Technologies | <input type="checkbox"/> ATE Hardware and Software              |
| <input type="checkbox"/> Reconfigurable Computing             | <input type="checkbox"/> Dependable HW / SW Systems             |
| <input type="checkbox"/> Network-based Collaborative Design   |   |

### Paper submissions:

Prospective authors are cordially invited to submit original papers using the symposium web page. Papers in English with a length of 6 pages maximum in IEEE conference style are expected. Special students and industrial sessions, as well as embedded mini-tutorials, will be organised by the symposium. Accepted papers will be included in the IEEE Symposium Proceedings and available through IEEE Xplore Digital Library.

### Important dates:

- Submission deadline: **January 9th, 2011**
- Notification of acceptance: **February 25th, 2011**
- Camera-ready deadline: **March 11th, 2011**

### Workshop location:

Lindner Congress Hotel, Berliner Platz, Cottbus, Germany

### DDECS contact address:

Heinrich T. Vierhaus  
Brandenburg University of Technology  
P. O. Box 10 13 44, D-03013 Cottbus, Germany  
[htv@informatik.tu-cottbus.de](mailto:htv@informatik.tu-cottbus.de)

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